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**END SEMESTER REGULAR/RETEST
EXAMINATION, JULY – 2023**

Branch : Computer

Semester : 4th (New)

Subject Code : CO 406

DIGITAL ELECTRONICS

Full Marks – 35

Time – Two hours

The figures in the margin indicate full marks for the questions.

Instructions :

- (i) All questions of PART – A are compulsory.
- (ii) Answer questions from PART – B as directed.

PART – A

Marks – 12

1. MCQ / Fill in the blanks/objective type :

(a) If the two inputs of a logic gate are 1 and 0, then the output of which logic gate is 1 ?

(i) AND gate

(ii) OR gate

(iii) NOR gate

(iv) NOT gate

[Turn over

(b) Which digital gate performs the multiplication operation ?

- (i) AND gate (ii) OR gate
(iii) NOR gate (iv) NAND gate

(c) Latches are _____ circuits.

- (i) Edge triggered (ii) Pulse triggered
(iii) Count triggered (iv) Level triggered

(d) Group of 4 bits forms

- (i) Byte (ii) Nibble
(iii) Gigabyte (iv) Terabyte

(e) R-S flip-flop has _____ inputs.

(f) A Ring counter has _____ flip-flops.

(g) Flip-flop is a _____ logic circuit.

(h) CD-ROM stands for _____.

(i) Registers and Counters are designed using _____.

(j) Adder is a _____ logic circuit.

(k) An _____ converts decimal numbers to binary and other codes.

(l) An _____ is also known as NOT gate.

PART - B

Marks - 23

Answer any two from (Q.No.2-4) and Q.No.5 is compulsory.

2. (a) Prove the following using Boolean Algebraic theorem : $AB+BC+B'C = AB+C$. 2

(b) Draw OR and AND gate using NAND gate only. 2+2=4

(c) Prove the following using Truth Table : $A+A'B = A+B$. 2

3. (a) Make the truth table for 3 input NOR gate. 3

(b) What are the differences between Combinational logic circuit and Sequential logic circuit. 5

4. (a) What is K-Map? 1
(b) List the advantages and disadvantages of K-Map. 4
(c) Define the laws of Boolean Algebra. 3
5. Write short notes on any two: $3.5 \times 2 = 7$
(a) Seven segment Display
(b) Full Adder
(c) TTL circuits
(d) LCD and LED Displays.